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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/639,071	08/11/2003	Kevin X. Zhang	42P7311C	6929

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EXAMINER

MCCARTHY, CHRISTOPHER S

ART UNIT	PAPER NUMBER
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2113

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07/25/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/639,071	ZHANG, KEVIN X.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-7 and 13-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 7 and 13-16 is/are rejected.
- 7) ☒ Claim(s) 6 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>response to arguments</u> . |

DETAILED ACTION

1. Claims 1-2, 5, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Partovi et al. U.S. Patent 5,353,424, as cited in prior office action, which was mailed on 2/8/07.
2. Claims, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partovi et al. in view of "Fail-Soft Circuit Design in a Cache Memory Control LSI" by Ooi et al, as cited in prior office action, which was mailed on 2/8/07.
3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Partovi as applied to claim 1 above, and further in view of Middleton et al. U.S. Patent 6,366,978, as cited in prior office action, which was mailed on 2/8/07.
4. Claims 6, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as cited in prior office action, which was mailed on 2/8/07.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-2, 5, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Partovi et al. U.S. Patent 5,353,424..

As per claim 1, Partovi teaches a processor comprising: a cache having a plurality of hit lines (column 2, lines 59-63) and a selector to provide a data during a clock cycle from a plurality of memory locations associated with the plurality of hit lines in the cache (column 4, lines 20-23; column 6, lines 19-42); a multi-hit detection circuit coupled to the hit lines to detect multiple hits in the cache during the clock cycle based on hit signals on the hit lines, the multi-hit detection circuit comprising a NAND gate with transistor pairs (column 11, lines 23-24); and an error flag generated by an inverter output in the multi-hit detection circuit during the clock cycle to indicate that the data provided during the clock cycle is invalid if multiple cache hits are detected, the error flag to indicate that the data provided during the clock cycle is valid if a single hit is detected (column 12, lines 15-22, wherein an error is occurred based upon redundant hits and this causes the device to produce a miss and no data is transferred and the gates are disabled; the inverter is used before the input of the NAND gate, but is indirectly used in the determination of the hits, and, therefore, is utilized in the generation of the error flag output; column 3, lines 6-8; wherein these same outputs can signal a valid hit).

As per claim 2, Partovi teaches the processor of claim 1, wherein the cache includes a plurality of comparators coupled to the hit lines to generate the hit signals based on comparisons between cache tags and a lookup tag (column 23-33).

As per claim 5, Partovi teaches the processor of claim 1, wherein the detection circuit includes a NAND gate having pull-down transistor pairs coupled to the hit lines to pull an output

node of the NAND gate low if two different hit signals indicate a hit (column 11, lines 23-40; column 12, lines 15-23, wherein the inverters are utilized in the determination of the of the redundant hits causing a false hit and thus producing a created error condition that results in the output of the NAND being a miss/low signal).

As per claim 7, Partovi teaches the processor of claim 5, wherein the cache is a multi-way set associative cache (column 1, lines 19-24).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partovi et al. in view of "Fail-Soft Circuit Design in a Cache Memory Control LSI" by Ooi et al.

As per claim 13, Partovi teaches a method of detecting multi-hit errors in a cache the method comprising: comparing a plurality of cache tags stored in each of a plurality of ways to a lookup tag to generate a plurality of hit signals during a clock cycle; selecting selected data from a plurality of memory locations, at least in part, on the plurality of hit signals during the clock cycle (column 4, lines 20-23; column 6, lines 19-42); comparing pairs of the plurality of hit signals during the clock cycle using a NAND gate with transistor pairs to determine if any two hit signals both indicate a multiple cache hit (column 11, lines 23-40); generating an error flag

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using an inverter output during a the clock cycle to indicate the invalidity of the selected data if the multiple hit is detected (column 12, 15-22, wherein an error is occurred based upon redundant hits and this causes the device to produce a miss and no data is transferred and the gates are disabled; the inverter is used before the input of the NAND gate, but is indirectly used in the determination of the hits, and, therefore, is utilized in the generation of the error flag output); and generating the error flag to indicate the validity of the selected data if the multiple cache hit is not detected (column 3, lines 6-8). Partovi does not explicitly teach wherein an indexed set. Ooi does teach an indexed set (section 3, ¶ 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the address index set of Ooi to the cache system of Partovi. One of ordinary skill in the art would have been motivated to combine the address index set of Ooi to the cache system of Partovi because Ooi teaches the suppression of false hit signals in a multi-hit cache system (section 3, ¶ 1); an explicit desire of Partovi (column 12, lines 16-26).

As per claim 14, Partovi teaches the method of claim 13, wherein comparing the plurality of cache tags includes comparing four cache tags of a four-way set associative cache to the lookup tag to generate four hit signals (column 1, lines 29-31, column 3, lines 31-35, wherein Partovi teaches his system to be on a 40way system and, therefore, would have 4 hits therein to utilize the multt-hit detection process).

As per claim 15, Partovi teaches the method of claim 14, wherein generating the error flag includes providing all pairings of the plurality of hit signals to gates of series-coupled pull-down transistor pairs of a NAND gate (column 12, lines 15-21).

As per claim 16, Partovi teaches the method of claim 13, wherein generating the error flag includes providing pairings of the plurality of hit signals to gates of series-coupled pull-down transistor pairs of a NAND gate.(column 12, lines 15-21).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Partovi as applied to claim 1 above, and further in view of Middleton et al. U.S. Patent 6,366,978.

As per claim 3, Partovi teaches he processor of claim 2. Partovi does not teach wherein the selector includes a multiplexer coupled to the hit lines to select data based on the hit signals. Middleton does teach wherein the selector includes a multiplexer coupled to the hit lines to select data based on the hit signals (column 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multiplexer of Middleton to the logic of Partovi. One of ordinary skill in the art would have been motivated to combine the multiplexer of Middleton to the logic of Partovi because Middleton teaches his multiplexer as a means in which to input multiple lines of a cache memory; an explicit desire of Partovi (figure 4, column 2, lines 63-64, wherein multiple inputs are used for comparing)..

Allowable Subject Matter

10. Claims 6, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims; wherein the inverters are coupled to the output nodes of the NAND gate. There is no motivation for Partovi to switch the inverters at his inputs of his NAND gate to the

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output of his NAND gate as this would not give him the desired delay time and not give him the proper results.

Response to Arguments

11. Applicant's arguments filed 5/7/07 have been fully considered but they are not persuasive.

With respect to claims 1 and 13, the applicant has amended the claims to include and has argued that Partovi does not teach the limitation of generating the error flag to indicate the data to be valid if a single hit is detected. The examiner respectfully disagrees. Partovi teaches that a miss condition is signaled when a multiple hit is detected (column 12, lines 18-21); that is, if both banks trigger outputs that indicate a hit, then a miss signal is accomplished. The examiner interprets this miss signal from the two positive hits in both banks as an indication that the data is not valid since two hits were detected. Likewise, if only one output from both banks indicates a hit, then the signal indicates a valid response and the data is valid (column 3, lines 4-8 teaches all the possible outputs among hits in a bank). Using the applicant's specification of page 11, the error flag indicates invalid data if the signal is high and the data as valid if the signal is low. The examiner correlates this to the table in Partovi in column 12, wherein if both banks indicate a hit, then the signals are high and the valid is not valid; likewise, if one signal is low and one is high, then that indicates a low signal and the data is valid; that is, if a hit is indicated, but not multiple hits are indicated, then the data is valid according to the output signal.

In light of the above arguments, and past arguments, all applicable rejected claims stand.

Conclusion

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Christopher S. McCarthy
Examiner
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